# MC3242A
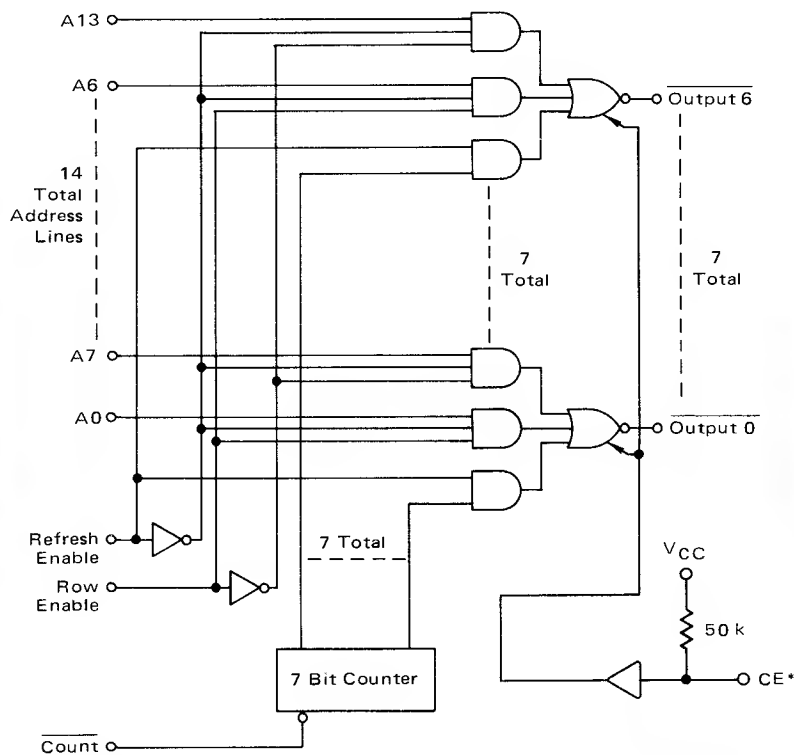
## MEMORY ADDRESS MULTIPLEXER FOR 16K RAMs

The Motorola MC3242A is an address multiplexer and refresh counter for 16-pin 16K dynamic RAMs that require a 128-cycle refresh. It multiplexes fourteen system address bits to the seven address pins of the memory device. The MC3242A also contains a 7-bit refresh counter that is clocked externally to generate the 128 sequential addresses required for refresh. The high performance of the MC3242A will enhance the high speed of the N-channel RAMs such as the MCM4116.

● Simplifies 16-Pin 16K Dynamic Memory Design
● Reduces Package Count
● 7-Bit Binary Counter for 128 Refresh Address
● Multiplexing: Row Address/Column Address/Refresh Address
● High Input Impedance for Minimum Loading of Bus:
  $I_F$ = 0.25 mA Max
● Schottky TTL for High Performance Address Input
    to Output Delay —
      $t_{AO}$ = 25 ns @ $C_L$ = 250 pF
● Second Source to Intel 3242
      (Detect Zero Function Not Included and Additional
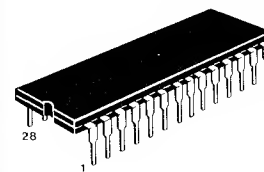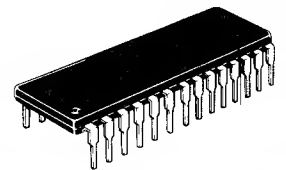      Chip Enable Feature Added at Pin 15)

## MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUITS

**L SUFFIX**
CERAMIC PACKAGE
CASE 733-03

**P SUFFIX**
PLASTIC PACKAGE
CASE 710-02

### LOGIC DIAGRAM



*See Pin Definitions

| Count | 1 | | 28 | $V_{CC}$ |
| Ref En | 2 | | 27 | A6 |
| Row En | 3 | | 26 | A13 |
| N.C. | 4 | | 25 | A5 |
| A1 | 5 | | 24 | A12 |
| A8 | 6 | | 23 | A4 |
| A2 | 7 | | 22 | A11 |
| A9 | 8 | | 21 | A3 |
| A0 | 9 | | 20 | A10 |
| A7 | 10 | | 19 | $\overline{O6}$ |
| $\overline{O0}$ | 11 | | 18 | $\overline{O3}$ |
| $\overline{O2}$ | 12 | | 17 | $\overline{O4}$ |
| $\overline{O1}$ | 13 | | 16 | $\overline{O5}$ |
| Gnd | 14 | | 15 | CE* |

Note:   A0 Through A6 Are Row Addresses
        A7 Through A13 Are Column Addresses
*See Pin Definitions

### TRUTH TABLE AND DEFINITIONS

| Refresh Enable | Row Enable | Output |
|---|---|---|
| H | X | Refresh Address (From Internal Counter) |
| L | H | Row Address (A0 through A6) |
| L | L | Column Address (A7 through A13) |

$\overline{Count}$ — Advances Internal Refresh Counter

◢ Indicates area of change from the previous issue.

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage | $V_I$ | −0.5 to +7.0 | V |
| Output Voltage | $V_O$ | −0.5 to +7.0 | V |
| Output Current | $I_O$ | 100 | mA |
| Operating Ambient Temperature | $T_A$ | 0 to +75 | °C |
| Storage Temperature | $T_{stg}$ | −65 to +150 | °C |
| Junction Temperature<br>  Ceramic Package<br>  Plastic Package | $T_J$ | <br>+175<br>+150 | °C |

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ $V_{CC}$ ≤ 5.5 V, 0°C ≤ $T_A$ ≤ 75°C; typical values apply with $V_{CC}$ = 5.0 V, $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Current, Low Logic State<br>  ($V_{IL}$ = 0.45 V) | $I_{IL}$ | — | −0.25 | −0.40 | mA |
| Input Current, High Logic State<br>  ($V_{IH}$ = 5.5 V) | $I_{IH}$ | — | — | 10 | μA |
| Input Voltage, Low Logic State | $V_{IL}$ | — | — | 0.8 | V |
| Input Voltage, High Logic State | $V_{IH}$ | 2.0 | — | — | V |
| Output Voltage, Low Logic State<br>  ($I_{OL}$ = 5.0 mA) | $V_{OL}$ | — | 0.25 | 0.4 | V |
| Output Voltage, High Logic State<br>  ($I_{OH}$ = −1.0 mA) | $V_{OH}$ | 3.0 | 4.0 | — | V |
| Input Clamp Voltage<br>  ($I_{IK}$ = −12 mA) | $V_{IK}$ | — | −0.8 | −1.5 | V |
| Power Supply Current<br>  ($V_{CC}$ = 5.5 V) | $I_{CC}$ | — | 80 | 125 | mA |

## SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ $V_{CC}$ ≤ 5.5 V, 0°C ≤ $T_A$ ≤ 75°C; typical values apply with $V_{CC}$ = 5.0 V, $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Propagation Delay Times<br>  Address Input to Output<br>    (Load = 1 TTL, $C_L$ = 250 pF)<br>    (Load = 1 TTL, $C_L$ = 15 pF, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $t_{AO}$ | <br><br>—<br>— | <br><br>12<br>6.0 | <br><br>25<br>9.0 | ns |
|   Row Enable to Output<br>    (Load = 1 TTL, $C_L$ = 250 pF)<br>    (Load = 1 TTL, $C_L$ = 15 pF, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $t_{OO}$ | <br>12<br>7 | <br>27<br>12 | <br>41<br>27 | ns |
|   Refresh Enable to Output<br>    (Load = 1 TTL, $C_L$ = 250 pF)<br>    (Load = 1 TTL, $C_L$ = 15 pF, $V_{CC}$ = 5.0 V, $T_A$ = 25°C) | $t_{EO}$ | <br>12<br>7 | <br>30<br>14 | <br>45<br>27 | ns |
| Count Pulse Width | $t_{W\overline{C}}$ | 30 | — | — | ns |
| Counting Frequency | $f_{\overline{C}}$ | 5.0 | 10 | — | MHz |

**FIGURE 1 — AC WAVEFORMS WITH MCM4116 NORMAL CYCLE**

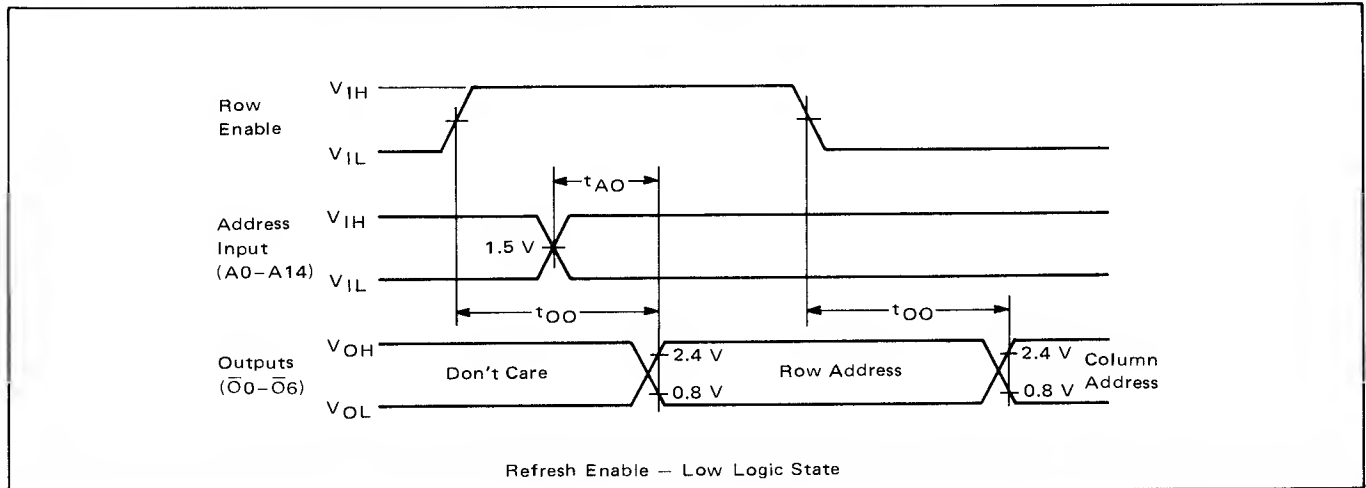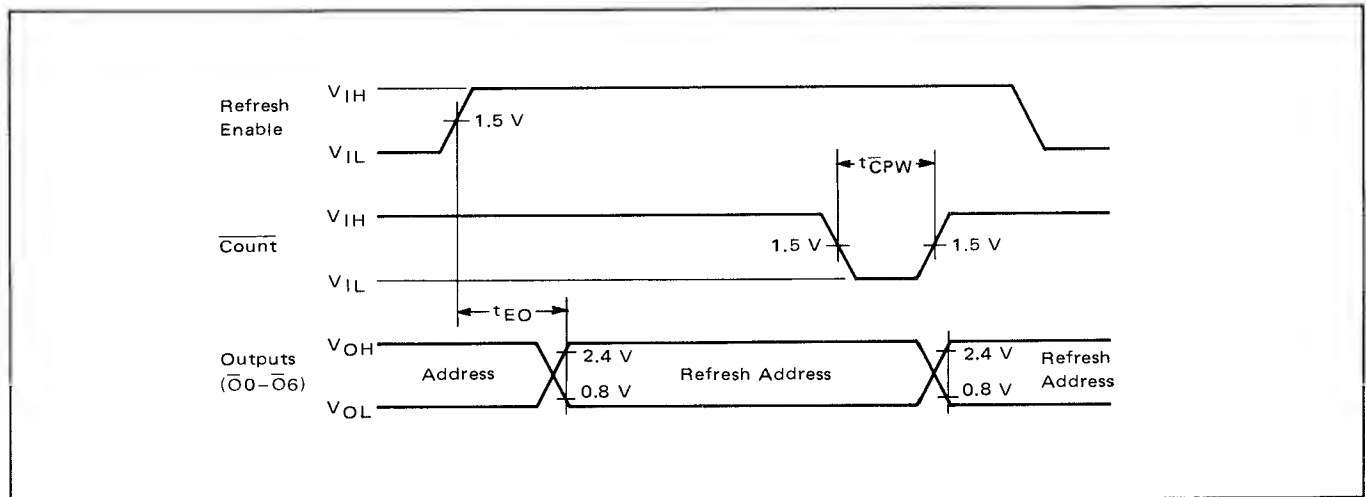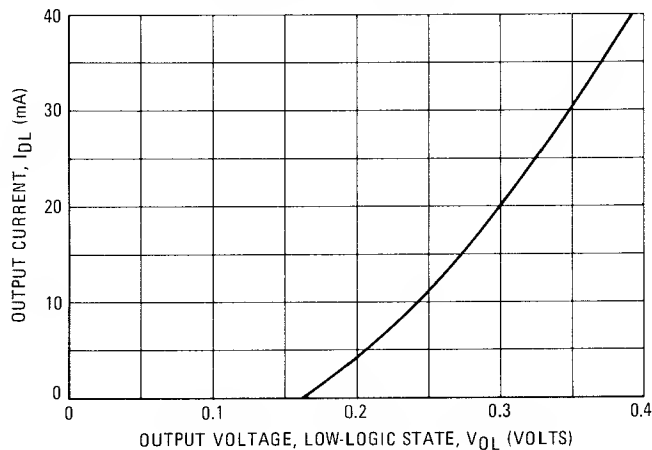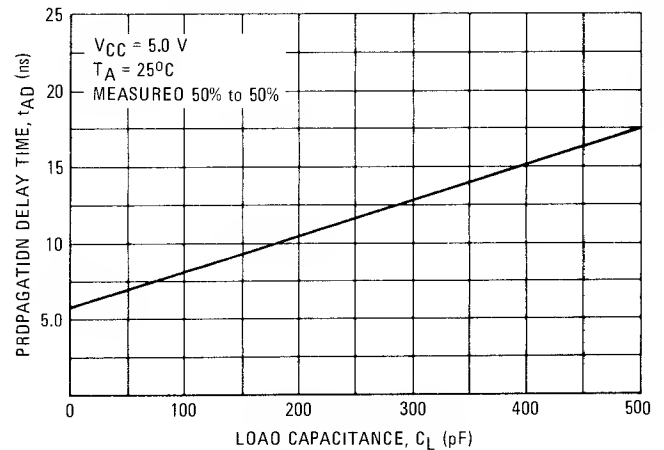

Refresh Enable — Low Logic State

**FIGURE 2 — REFRESH CYCLE**



## TYPICAL CHARACTERISTICS

**FIGURE 3 — OUTPUT CURRENT versus OUTPUT LOW VOLTAGE**



**FIGURE 4 — PROPAGATION DELAY versus LOAD CAPACITANCE**
Row or Column Address to Output



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# PIN DEFINITIONS

$\overline{\text{Count}}$ **Input — Pin 1**

Active low input increments internal 6-bit counter by one for each count pulse in.

**Refresh Enable Input — Pin 2**

Active high input which determines whether the MC3242A is in refresh mode (H) or address enable (L).

**A0–A6 Inputs — Pins 9, 5, 7, 21, 23, 27**

Row address inputs.

**A7–A13 Inputs — Pins 10, 6, 8, 20, 22, 24, 26**

Column address inputs.

**$\overline{\text{O}}$0–$\overline{\text{O}}$6 Outputs — Pins 11, 12, 13, 18, 17, 16, 19**

Address outputs to memories. Inverted with respect to address inputs.

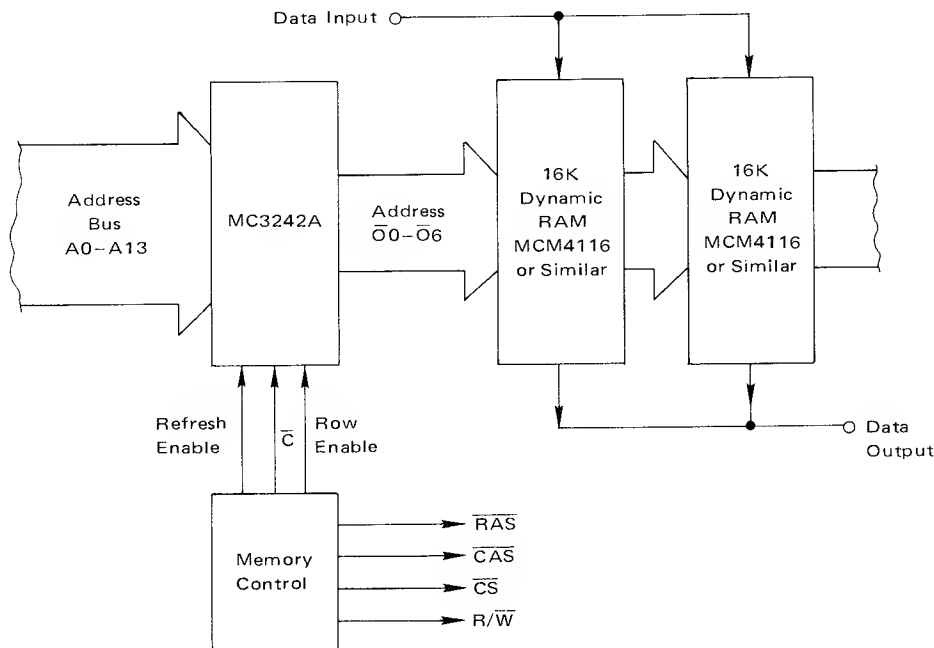**Gnd — Pin 14**

Power supply ground.

**CE Input — Pin 15**

Optional use, chip enable control pin. Left open, an internal 50 k$\Omega$ pullup resistor keeps this pin high and the MC3242A is a functional replacement for the Intel 3242 (without detect zero function). As an active input, when pulled low, all 3242A outputs go three-state.
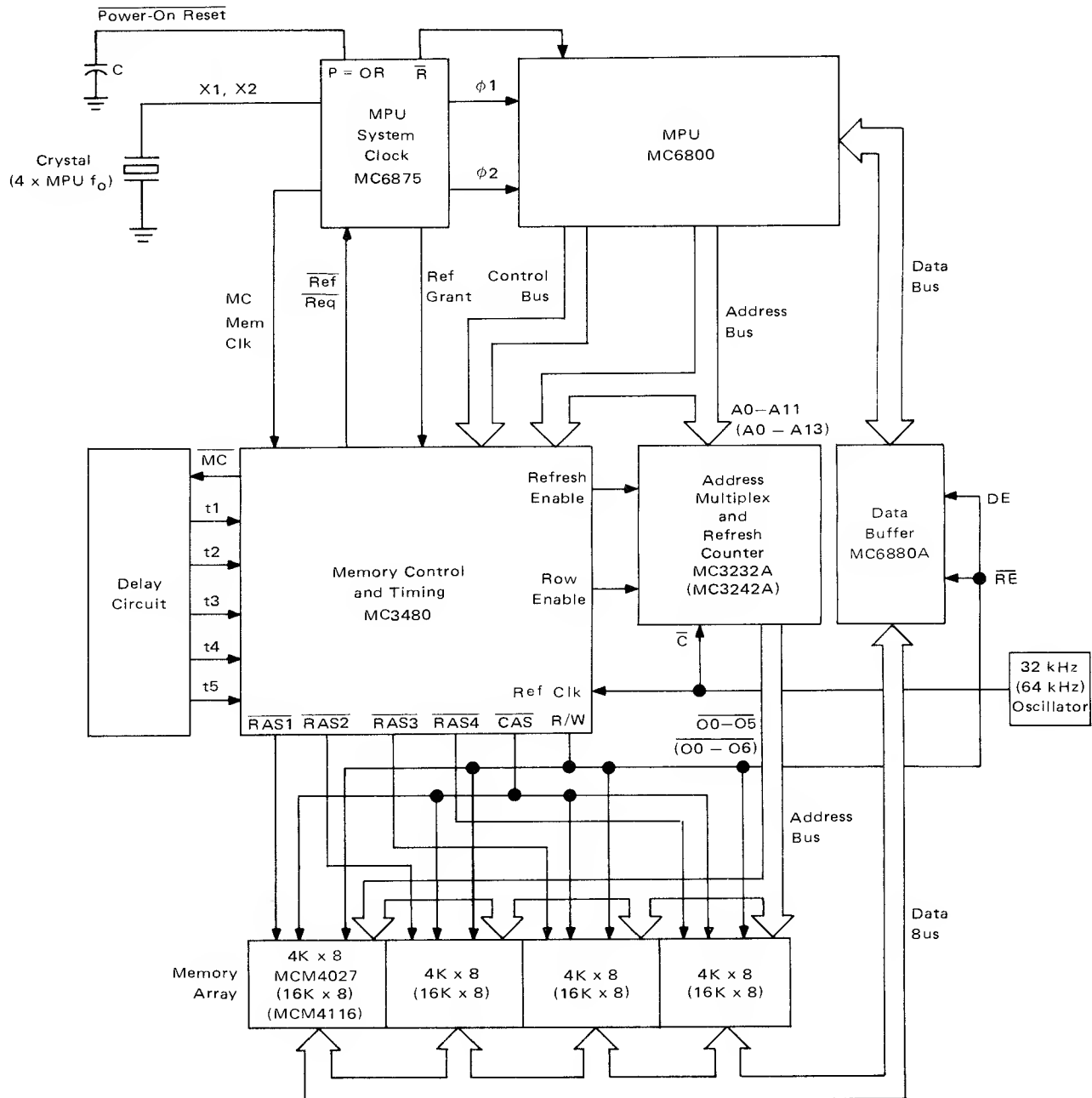
**V$_{CC}$ — Pin 28**

+5 V power supply input. Due to high capacitance drive capability, a 0.1 $\mu$F capacitor should be used to ground along with careful V$_{CC}$ and Gnd Bus layout.

**GENERAL 16K DYNAMIC RAM
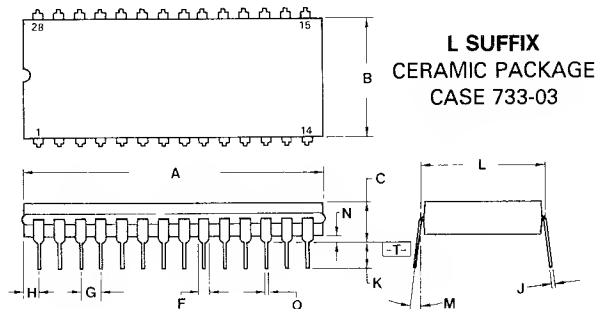SIMPLIFIED BLOCK DIAGRAM**



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# TYPICAL APPLICATION
## 16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate
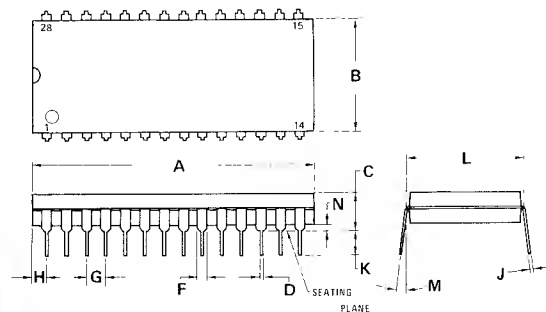part types or values for 16K x 1 RAMs



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## OUTLINE DIMENSIONS

**L SUFFIX**
CERAMIC PACKAGE
CASE 733-03

**P SUFFIX**
PLASTIC PACKAGE
CASE 710-02

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 36.45 | 37.21 | 1.435 | 1.465 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 36.45 | 37.85 | 1.435 | 1.490 |
| B | 12.70 | 15.37 | 0.500 | 0.605 |
| C | 4.06 | 5.84 | 0.160 | 0.230 |
| D | 0.38 | 0.56 | 0.015 | 0.022 |
| F | 1.27 | 1.65 | 0.050 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 5° | 15° | 5° | 15° |
| N | 0.51 | 1.27 | 0.020 | 0.050 |

NOTES:
1. DIM [A] IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   [⊕] Ø 0.25 (0.010) Ⓜ T A Ⓜ
3. [T] IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

## THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

$T_A$ = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

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